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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/218,997 12/22/98 FUKAMI

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EXAMINER

IM52/0618

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ART UNIT

PAPER NUMBER

1744

DATE MAILED:

06/18/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

**Office Action Summary**

Application No.

09/218,997

Applicant(s)

FUKAMI, TERUAKI

Examiner

Imad Soubra

Art Unit

1744

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 June 2001.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☒ All b) ☐ Some \* c) ☐ None of the CERTIFIED copies of the priority documents have been:
1. ☐ received.
2. ☐ received in Application No. (Series Code / Serial Number) \_\_\_\_\_.
3. ☒ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

**Attachment(s)**

- 15) ☐ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 18) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other:

## DETAILED ACTION

**This action is made final.**

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

- Determining the scope and contents of the prior art.
- Ascertaining the differences between the prior art and the claims at issue.
- Resolving the level of ordinary skill in the pertinent art.
- Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1-5, 12, 14-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashida et al in view of Suzuki et al. Hayashida intrinsically discloses a similar solution that is used to treat silicon wafer. Hayashida teaches that the RCA cleaning method is a combination of (I) SC-1 treatment using ammonia hydrogen peroxide and water and effective for removing contamination with organic materials and a part of metals such as Cu, Ag, etc (column 1, lines

25-29). The reference teaches that if Cu is part of the solution, then the contaminants will be removed from the wafer. The reference teaches that the metallic elements detected on the surface of wafer after the SC-1 treatment are Fe, Al, Ca, Mg, Zn, etc (column 1, lines 57-61). The reference discloses the amount of Fe concentration in the SC-1 solution also associating that with the concentration of copper as well. So the reference teaches that the concentration is necessary in maintaining the electrical properties after SC-1 cleaning, it is necessary to maintain the Fe (which also relates to the concentration of copper intrinsically) concentration in the SC-1 treating solution at 0.01 ppb or less (column 4, lines 43-45) which this concentration is notoriously well known in the art for the use of metals in chemical solution when treating silicon wafer. Hayashida et al further teaches that a wafer with metallic impurities and there arised the problems in electrical properties such as deterioration in oxide breakdown voltage and recombination lifetime, etc (column 1, lines 52-56). In addition, the patent of Hayashida et al teaches that a step of treating surfaces of semiconductors with a surface treatment solution comprising an inorganic or organic alkali, hydrogen peroxide and water as major components and a step of treating (or rinsing) the resulting surfaces with ultra-pure water, at least one of the surface treating solution and the ultra-pure water containing as a complexing agent a compound having one or more phosphoric acid groups or a salt thereof in the molecule and showing chelating ability or an oxidized form thereof and so on (column 3, lines 28-36). Also, the reference teaches that various known chelating agents in an amount of  $10^{-4}$  by weight were added to a SC-1 cleaning

solution containing 1 ppb of Fe to compare adsorbed amounts of Fe on silicon wafer surfaces; in the case of using EDTA, (CyDTA), (TTHA), and (NTA), these having almost the same high complex-formation constant for Fe, the adsorbed amounts were reduced to only about  $\frac{1}{2}$  to  $\frac{1}{3}$  of the case of adding no chelating agent (column 5, lines 1-11). The reference also teaches that the semiconductor surface treating solution of the present invention may further contain one or more various auxiliaries such as surfactants, etc, so long as the effects of the present invention are not damaged (column 8, lines 11-14). On the other hand, the patent of Hayashida et al fails to disclose the method of storing and water storage for silicon wafers. However, Suzuki et al intrinsically disclose a similar method in using purified water for storage of semiconductors. Suzuki et al teaches that in the fabrication of mirror wafers from wafers cut from a single crystal silicon rod, the said wafers are generally treated in the processes of chamfering, lapping, washing, etching, prewashing for annealing, and annealing and so on (column 1, lines 22-24). The Suzuki et al further teaches that the object of the invention is to provide a method for the storage of wafers in process, which method, for the purpose of preventing the contamination of surfaces of wafers which frequently occurs particularly during the storage of wafers which frequently occurs particularly during the storage of wafers after the treatment with a chemical liquid among other processes for the production of wafers, adopts a relatively simple measure of temporarily storing the wafers in an aqueous hydrogen peroxide solution instead of the conventional measure of temporarily storing them in purified water or storing them in a clean dry air

(column 3, lines 14-26 and column 5, lines 18-34). So it is notoriously well known in the art to store semiconductors in water with concentration of 0.01 ppb of Cu. The teaching is also discussed as admitted art in the applicant's specification on page 2, paragraph 3 where it states "Generally, ultrapure water is used as such water for storing a silicon wafer, so as not to contaminate the wafer". The motivation for combining the two references would be to show that the same water used for cleaning can also be used for storage, which is an obvious substitution. Clearly, combining the two references will reveal the same limitation as the applicant is claiming. Therefore, it would have been obvious of one having ordinary skill in the art at the time the invention was made to incorporate the same water used for cleaning into storing silicon wafers in order to effectively preserve a silicon wafer and to save on labor costs (column 1, lines 31-46).

2. Claims 6-7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashida et al in view of Suzuki et al as applied to the claims above, and further in view of Kern. However, both references do not disclose silicon wafer having a hydrophobic surface. Kern teaches this in his reference in detail on page 402. The teaching is that a contact angle of 180 degrees defines a completely hydrophobic surface (page 402, lines 3-4). Clearly, the description used to teach the hydrophobic behavior is certainly well known in the art. Further, the motivation for combining the references is to illustrate the behavior of silicon wafer of not liking water. Therefore, it would have been obvious of one

having ordinary skill in the art at the time the invention was made to include the non attractive behavior of silicon wafer towards water in order to show that the contaminants in the water are not on the wafer (page 402, lines 10-12).

3. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashida et al in view of Suzuki et al and Kern as applied to the claims above, and further in view of Gill et al. The references above fail to disclose the method of storing wafers into water immediately after polishing. However, the patent of Gill et al intrinsically teaches this method in detail. Gill teaches that Figure 14 is a section view illustrating operation of the wafer water track assembly to transport a wafer from the polishing head to a water cassette wherein the wafer are being stored; and Figures 15A to 15E illustrate operation of the wafer transport head assembly to remove a wafer from the wafer dolly and position the wafer adjacent the polishing head (column 3, lines 10-16). Clearly, the motivation for combining the references is to prevent the wafer from being contaminated from impurities (see entire reference). Therefore, it would have been obvious of one having ordinary skill in the art at the time the invention was made to incorporate the method of storage after the wafer has been polished in order to preserve the wafer.

4. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashida et al in view of Suzuki et al as applied to the claims above, and further in view of Ilardi et al. The references above fail to disclose that the chelating

agent has a chelate compound production performance not lower than that of NTA. However, Ilardi et al intrinsically disclose this by providing an example that one can be substituted for the other. Ilardi et al teaches that the metal removal capabilities of a cleaner formulation for the removal of aluminum, copper, and iron from metal contaminated silicon wafers; cleaner formulation A was prepared by dissolving EDTA and so on; cleaner formulation B was similarly prepared substituting NTA for the EDTA and they both achieve the same results according to the reference (column 10, line 59-column 11, line 7).

#### ***Applicants Arguments***

5. The solution of Hayashida is used only to treat a surface of a wafer, but is not used to store a wafer in storage water.
6. The reference does not describe the problem described at line 11 of page 3 through line 4 of page 4 of the present application that even if contaminants are removed from a surface of a wafer by cleaning, degradation of oxide dielectric breakdown voltage occurs when storing a wafer.
7. Hayashida describes a cleaning solution containing Fe at a concentration of 0.01ppb or less, but does not describe a cleaning solution containing Cu at a concentration of 0.01ppb or less.



8. Suzuki et al does not describe that wafers are stored in purified water containing Cu at a concentration of 0.01ppb or less and that wafers are stored in a chemical solution with an added chelating agent.

9. Suzuki et al neither describes nor suggests a method for adding a chelating agent to storage water.

***Response to Applicants Arguments***

5. The patent of Suzuki et al teaches the method of storing silicon wafers (column 1, lines 9-11).

6. The claims are written in open language and do not preclude any additional elements or additional steps. The claims do read on the references as stated above in the Examiner's rejection statements.

7-9. The applicant states that the water contains Cu at a concentration of 0.01ppb or less in which the Examiner can interpret the concentration of Cu to be at 0. Cu is not an essential limitation since the range can be from 0 to 0.01ppb of Cu in water for the storage of silicon wafers.

Application/Control Number: 09/218997

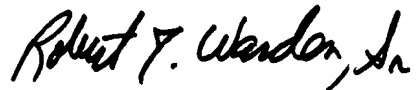
Art Unit: 1744

***Conclusion***

Any inquiry concerning this communication from the examiner should be directed to Imad Soubra whose telephone number is (703) 305-3541. The examiner can normally be reached on 8:30 am to 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Warden can be reached on (703) 308-2920. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3599 for regular communications and (703) 305-5408 for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1193.

Imad Soubra

February 21, 2001



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